WHAT IS CLAIMED IS:

1. A data processing system, comprising:

at least one main processor connected to a system bus;

a system memory connected to the system bus and accessible to each of the processors;

error logic configured to receive internal error signals asserted by one or more of the main processors and to respond to an internal error signal by disabling the processor asserting the signal and restarting the system with any remaining functional processors.

2. The system of claim 1, wherein the error logic is further configured to record the internal error signal in an error status register of the error logic.

3. The system of claim 2, wherein the error status register includes at least a pair of bits corresponding to each of the main processors, wherein a first bit of each pair is indicative of whether the corresponding main processor is currently asserting its internal error signal and a second bit of each pair is indicative of whether the corresponding main processor has asserted its internal error signal previously.

4. The system of claim 1, wherein the error logic is functional substantially immediately following the application of power to the data processing system.

5. The system of claim 1, wherein the error logic includes an error detection unit configured to receive an internal error signal from each of the main processors and further configured to generate an error detect signal responsive to assertion of an internal error signal by any of the processors.

6. The system of claim 5, wherein the error logic further includes error logging logic configured to receive the error detect signal and, responsive thereto, to update an error status register to reflect the internal error signal.

7. The system of claim 6, wherein the error logic is further configured to generate a service processor interrupt responsive to error status register update.

8. The system of claim 7, wherein the data processing system further includes a service processor configured to receive the service processor interrupt from the error logic.

9. The system of claim 8, wherein responsive to the service processor interrupt, the service processor is configured to powering down the system.

10. Error detection logic suitable for use in a data processing system, wherein the error detection logic is configured to receive internal error signals asserted by one or more main processors of the data processing system and further configured to respond to an internal error signal by disabling the processor asserting the signal and restarting the system with any remaining functional processors.

11. The error logic of claim 10, wherein the error logic is further configured to record the internal error signal in an error status register of the error logic.

12. The error logic of claim 11, wherein the error status register includes at least a pair of bits corresponding to each of the main processors, wherein a first bit of each pair is indicative of whether the corresponding main processor is currently asserting its internal error signal and a second bit of each pair is indicative of whether the corresponding main processor has asserted its internal error signal previously.

13. The error logic of claim 10, wherein the error logic is functional substantially immediately following the application of power to the data processing system.

14. The error logic of claim 10, wherein the error logic includes an error detection unit configured to receive an internal error signal from each of the main processors and further configured to generate an error detect signal responsive to assertion of an internal error signal by any of the processors.

15. The error logic of claim 14, wherein the error logic further includes error logging logic configured to receive the error detect signal and, responsive thereto, to update an error status register to reflect the internal error signal.

16. The error logic of claim 15, wherein the error logic is further configured to generate a service processor interrupt responsive to error status register update.

17. A method of handling internal errors in a data processing system, comprising:

detecting internal error signals asserted by one or more main processors of the data processing system;

responsive to detecting the internal error signals, updating an error status register to reflect the assertion of any of the error signals;

disabling one or more of the main processors based on the contents of the error status register; and

restarting the system with the remaining processors.

18. The method of claim 17, wherein updating the error status register includes updating a current status bit for each of the main processors based on the current state of the corresponding internal error signal.

19. The method of claim 18, wherein updating the error status register further includes updating cumulative status bits for each of the main processors to reflect historical assertion of the error status signal of the corresponding processors.

20. The method of claim 17, further comprising, responsive to detecting the assertion of one or more of the error status signals, issuing an interrupt to a service processor of the data processing system.